A Compensated Linearity Voltage-Control-Capacitor Device by Standard CMOS Process

TECHNICAL FIELD

[0001] The present invention relates to varactor (or voltage controlled capacitors) devices and more specifically to a varactor using a multiplicity of parallel back-to-back CMOS devices to provide a large capacitance range over a large and substantially linear voltage range.

BACKGROUND

[0002] The capacitance and/or frequency of a varactor or Variable Voltage Capacitor varies directly as the applied voltage varies, and consequently finds significant application with oscillator circuits such as used in communication devices. As an example, an oscillator circuit that is controlled by a varactor offers high-speed operation, low noise and low power consumption. The operating frequency of such an oscillator can be controlled or tuned by varying the voltage across the terminals of the varactor and, therefore, ideally the varactor will have a high maximum to minimum capacitance ratio. This is because the difference between the maximum and minimum capacitance over the full range of the controlled voltage will be proportional to the tuning range of the oscillator. Thus, a large capacitance range results in a large tuning range of the oscillator. The ideal variable voltage capacitor will also operate substantially linearly over a large voltage range such that the oscillator changes its operating frequency smoothly over a large voltage range.

[0003] FIG. 1A illustrates the circuit schematic of an ideal LC oscillator (inductive capacitance) voltage controlled variable circuit or varactor, and FIG. 1B illustrates a linear relationship between the applied voltage V_C (on the horizontal axis 10) and the operating

frequency Hz of the oscillator (on the vertical axis 12). Unfortunately, as will be appreciated by those skilled in the art, semiconductor varactors or Variable Voltage Capacitors, simply do not demonstrate such a linear relationship.

[0004] Prior art semiconductor varactors are primarily of two types: a PN-junction varactor and a MOS varactor. The PN-junction varactor has the advantage that it can be implemented in a standard CMOS semiconductor process. Unfortunately, the PN-junction has a low maximum to minimum capacitance ratio, which, of course, as discussed above limits the operating frequency range of an oscillator using such a PN-junction varactor. On the other hand, a MOS varactor, such as shown in the semiconductor structure diagram of FIG. 2A and the electrical schematic of the back-to-back pair of varactors shown in FIG. 2B has an acceptable capacitance ratio, but the transition from the minimum C_1 to the maximum C_2 as shown in the graph of FIG. 2C from maximum to minimum or minimum to maximum, and as will be discussed later, is very abrupt over a small gate voltage (Vg) range V_1, V_2 such that the device is very non-linear.

[0005] One attempt to achieve the goal is described in U.S. Patent 6,407,412 entitled "MOS Varactor Structure with Engineered Voltage Control Range" and issued to Krzysztof Iniewski, *et al.* on June 18, 2002. However, the device requires a somewhat complicated process flow to provide the necessary P+ and N+ parallel-connected regions.

[0006] Therefore, it would be advantageous to provide a semiconductor varactor having a large capacitance ratio, which varies linearly over a large input voltage and can be manufactured by using standard CMOS processing.

SUMMARY OF THE INVENTION

[0007] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by embodiments of the present invention, which describes a method of forming a semiconductor varactor device having improved linearity. The method comprises the following steps. The device is formed on a semiconductor substrate and includes forming at least first and second differential varactor elements. Each of the differential varactor elements formed on the semiconductor substrate comprises forming first, second and third N+ doped regions in an N well and forming a first gate for controlling the first and second N+ doped regions and forming a second gate for controlling the second and third N+ doped regions. In addition, a first resistor is also formed on the semiconductor substrate to be connected to and receive power from a selected voltage source. The first resistor is formed so that after the first, second and third N+ doped regions of the first differential varactor elements receive power from the voltage source, the first, second and third N+ doped regions of the second differential varactor elements are connected to the other end of the first resistor such that there is a voltage drop across the first resistor before the power reaches the second differential varactor elements. According to one embodiment, the first and second gates are formed as N-type gates.

[0008] Although the forming of first and second (or two) differential varactor elements connected in parallel may be used to manufacture an improved oscillator according to this invention, it should be appreciated that even better linearity over a wider range of voltages may be achieved by using three or more differential varactor elements connected in parallel. That is, as many differential varactor elements as necessary may be connected in parallel according to the present invention so long as a series of resistors are also formed to control the bulk voltage of the

regions of the differential varactor elements by connecting the resistors to provide a series of different voltage drops.

[0009] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0011] FIG. 1A illustrates the circuit schematic of an LC oscillator with ideal voltage controlled capacitor or varactor;

[0012] FIG. 1B illustrates the linear relationship between the applied voltage V_C on the horizontal axis and the operating frequency Hz of the varactor on the vertical axis;

[0013] FIG. 2A is a prior art semiconductor structure portion of a single stage varactor;

[0014] FIG. 2B is an electrical schematic of an oscillator with a pair of back-to-back varactors having the prior art structure of FIG. 2A;

[0015] FIG. 2C is a graph illustrating the steep rise in capacitance with respect to voltage changes of the varactor of FIGs. 2A and 2B;

[0016] FIG. 3A illustrates electrical schematics of three varactors of the prior art semiconductor structure of FIG. 2A having three different bulk bias voltages applied to the structure;

[0017] FIG. 3B shows the three steep capacitance vs. voltage curves of the circuits of FIG. 3A as solid line graphs;

[0018] FIG. 3C is an electrical schematic of the three circuits of FIG. 3A connected in parallel;

[0019] FIG. 4A is a cross-sectional view of a semiconductor structure of back-to-back varactors according to the present invention and having a capacitance voltage output similar to that shown in FIG. 4D;

[0020] FIG. 4B is a top view of the semiconductor structure of FIG. 4A;

[0021] FIG. 4C is an electrical schematic illustrating the semiconductor structure of FIGs. 4A and 4B of a plurality of back-to-back varactors according to the present invention; and

[0022] FIG. 4D is a graph illustrating the idealized resulting capacitance to voltage curve achieved by the present invention when a plurality of different optimized voltages are applied to the bulk region of the electrical schematic of FIG. 4A.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0023] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0024] Referring again to FIG. 2A, there is shown a semiconductor variable capacitance circuit that may be used in an oscillator circuit. As shown, a standard CMOS process is used except that an N well 14 is formed in the semiconductor 16 rather than the typical P well. This may be achieved by simply changing the P well implant mask to an N well implant mask. N well 14 includes a couple of N+ regions 18a and 18b that are connected together to a voltage or bulk voltage source 20. A gate member 22 is formed between the N+ regions 18a and 18b such that a voltage can be applied to the gate 22 to control the operation of the circuit.

[0025] Referring to FIG. 2B, there is shown an LC oscillator circuit, which includes two of the circuits shown in FIG. 2A and identified in the circuit of FIG. 2B as circuits 24a and 24b. As shown, these circuits are connected as back-to-back differential varactor circuits with the bulk voltage V_C being applied to terminal 26. Therefore, as will be appreciated by those skilled in the art, when the back-to-back varactor elements are connected in parallel to an inductive element, such as inductive elements 28a and 28b, an LC circuit having a linear portion is provided. The variable capacitance of the circuit of the device shown in FIG. 2B is illustrated in FIG. 2C. As can be seen, a graph of the capacitance vs. voltage of such a circuit has a linear area 30 of capacitance change between a small voltage change 40 between voltages V_1 and V_2. At each

side of the linear change 30, however, there is very little change in the capacitance with increase in voltage as seen in areas 41a and 41b. As was discussed before, it is desirable for an oscillator used in communications to have a variable capacitor that varies substantially linear over a wide range of voltages. Such a linear change over a wide voltage range allows for easy tuning of a communication circuit. Therefore, although the graph indicates a linear area 30 in FIG. 2C, the change in capacitance occurs over the very small voltage range (between V_1 and V_2), which makes it difficult to provide discrete changes in the capacitance.

[0026] Various attempts have been made to solve this problem. For example, referring to FIG. 3A there is shown three circuits of the type discussed above with respect to FIG. 2A and FIG. 2B except that the bulk voltage V of each of the three circuits is different as indicated at V_1, V_2 and V_3.

[0027] The solid line curves 42a, 42b and 42c of FIG. 3B illustrate how the voltages for the three circuits of FIG. 3A are optimally selected.

[0028] Referring to FIG. 3C, there is illustrated an electrical schematic of three circuits 43A, 43B and 43C similar to those of FIG. 3A connected in parallel according to the present invention. As discussed above, the solid line graphs of FIG. 3B illustrate the different outputs of the three circuits 43a, 43b and 43c of FIG 3C when the voltages V_1, V_2 and V_3 are optimally selected. The dashed line curve 44 of FIG. 3B illustrates the combined outputs of the three circuits when the voltages V_1, V_2 and V_3 are optimally selected and the circuits are connected in parallel.

[0029] Referring now to FIGs. 4A and 4B, there are shown a cross-sectional view and a top view of a semiconductor structure incorporating the teachings of the present invention. As shown, the structure is built upon a P-type substrate 50, which, according to the present

embodiment, includes four N well areas 52a, 52b, 52c and 52d. Each of the N wells includes a first region 54, a second region 56 and a third region 58 all of which are N+ regions within the N wells 52a – 52d. Silicon oxide areas 60 are shown separating each of the N wells 52a – 52d. A first gate 62 above each of the N wells will control the electron flow between the first and second N+ regions 54 and 56 whereas a second gate 64 will control electron flow between the second and third regions 56 and 58. All of the first gates 62 are connected in parallel and have a common output terminal 66. Likewise, each of the second gates 64 is also connected in parallel and have a common output terminal 68. Further, although the above discussions, as well as the following discussions are with respect to N well varactors, it is also possible to include a PMOS-like varactor by forming P+ doped regions in a P well with first and second gate members.

[0030] There is also included a group of resistors 70a, 70b, 70c, 70d and 70e, connected in series as is better shown in FIG. 4B. These serially connected resistors, as will be discussed hereinafter, provide a series of voltage drops so that each of the N wells 52a – 52d has a different bulk voltage. This can be seen better in FIG. 4B wherein a voltage terminal 72 receives voltage from a voltage source, not shown, and this voltage is provided to the bulk region of N well 52a as shown by the connections 74a more clearly seen in FIG. 4B. The resistor 70a is also connected to the voltage source 72 and, in turn, it creates a voltage drop such that a second and lower voltage is provided to the N well 52b as indicated by electrical connections 74b. A second resistor 70b provides a second voltage drop to the N well 52c by the connections 74c. In a similar manner, resistors 70c, 70d and 70e provide additional voltage drops to the N well 52d and any other N wells. Resistors 70d and 70e illustrate that other additional N wells may be included in the circuitry. It is also possible of course, that another resistor be included between the voltage source 72 and the first bulk region 52a, such as resistor 76 shown in dashed lines in

FIG. 4B to drop the voltage from that received from source 72 before it is applied to the first N well 52a.

[0031] Therefore, referring now to FIG. 4C, there is shown an electrical schematic of a plurality of back-to-back varactors of the type shown in FIGs. 4A and 4B and similar to that of FIG. 3C, except that there is included the resistors 70a, 70b, 70c, 70_N and 76 for providing voltage drops such that each of the back-to-back differential varactors is operating at a different bulk voltage. Consequently, if these resistors are optimally selected to provide specific voltage drops, the plurality of back-to-back vectors connected in parallel will generate a capacitance to voltage output similar to curve 44 shown in FIG 4D.

[0032] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

[0033] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.